Energy Aware Task Mapping Algorithm For Heterogeneous MPSoC Based Architectures

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***Abstract*—Energy Management for multi-mode Software Defined Radio (SDR) systems remains a daunting challenge. In this paper, we focus on the issue of task allocation for multi-processor based systems with hybrid processing resources that can be reconfigured. With the objective of minimizing energy, we propose a fast, energy aware static task mapping heuristic to minimize the average overall energy consumption. Simulation results show that the proposed heuristic is capable of achieving results that are within 20% of the optimal solution while providing orders of magnitude speedup in processing time.**

I. Introduction

With the current advances in wireless communication and the limitations of spectrum access, future wireless networks are steadily progressing to a co-operative model aiming to provide universal coverage that implicitly encapsulates nodes that can support multiple Radio Access Technologies (RATs). Examples are IEEE 802.21 and IEEE P1900.4 standards. To fully benefit from such emerging network concepts, there is a need for efficient design time and run time reconfigurable platforms. Numerous reconfigurable architectures have been proposed spanning different technologies including application specific instruction set processors (ASIPs), field programmable gate arrays (FPGAs), and digital signal processors (DSPs). Recently, multi-processor systems on chip (MPSoC) architectures have evolved rapidly in the race of high performance embedded computing [1], especially in applications that require a flexible computing structure that can be reconfigured to handle various applications. A common design metric among all platforms is reducing energy consumption that restricts both the capabilities of the device and the design choices that are available. Towards that end, numerous techniques have been developed to optimize energy consumption at different levels including algorithm, system, architecture, and circuit levels.

A main factor that impacts energy consumption in MPSoC based architectures is task allocation [2]. Several task allocation and scheduling techniques have been proposed in literature such as [3] and [4] for homogeneous and heterogeneous MPSoCs. Some consider real time tasks, and some consider dynamic voltage scaling (DVS)with task allocation and scheduling.

This work extends the original work in [5], which proposed the static and dynamic task mapping approaches for probabilistic applications based on static and dynamic power components. This extension considers only the static mapping and takes into account the communication and reconfiguration energy componentshich has a significant contribution to the overall energy consumption [6] and [7].

The paper is organized as follows: Section II summarizes the extended system model. The proposed heuristic solution is presented in section III followed by the performance results in section IV. Section V concludes the paper.

II. System Model

We assume a generic heterogeneous MPSoC architecture with different types of processing units (PUs). Each PU can run more than one task simultaneously based on its computational capability and the computational requirements of these tasks. The PUs are communicating through available means of on chip communications. We assume a simple 2D grid network model connecting different PU instances. The system can have multiple applications (scenarios), each one is characterized with a certaion probability , and is represented by a task graph. When a certain application comprising a set of tasks starts to run on the platform, the tasks are mapped to different PUs, as depicted in Figure 1 based on a mapping procedure, and the selected PUs are configured to perform the corresponding tasks.

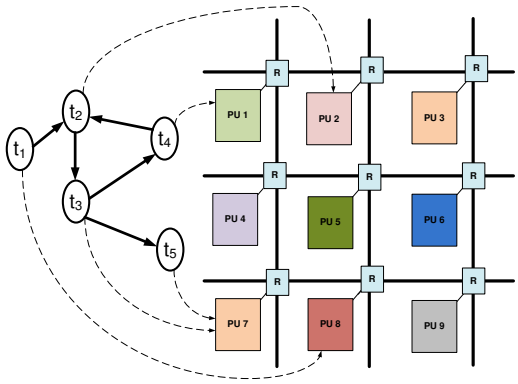

Fig. 1. Application to architecture mapping

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III. Proposed Mapping algorithm

The target is to find the optimal task mapping that minimizes the overall average energy consumption. The problem is formulated as a binary quadratic programming (BQP). We propose an iterative heuristic solution that approaches the optimal binary quadratic programming solution. The algorithm flow is shown in Figure 2. In this solution, the estimated energy consumption for each task is updated at each iteration. The solution converges with the increase of number of iterations to approach the optimal solution.

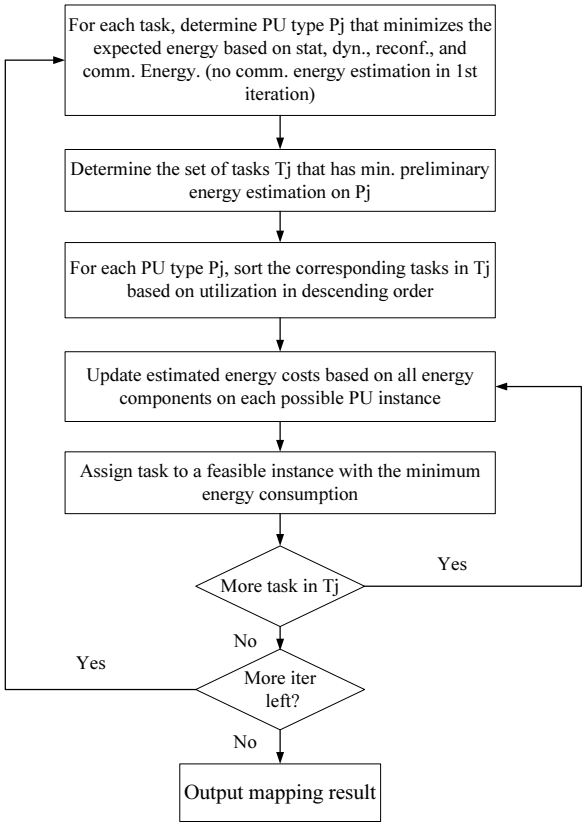


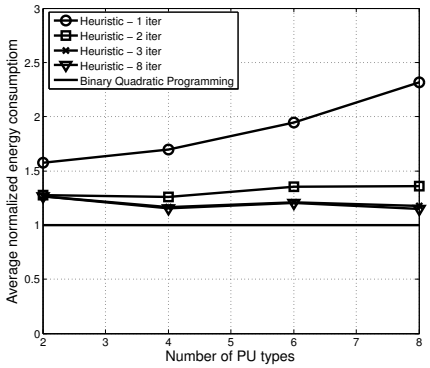
Fig. 2. Mapping heuristic flowchart

IV. Performance Results

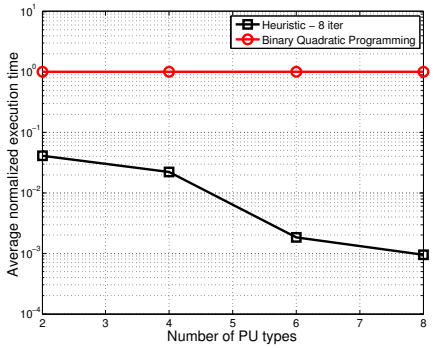
To demonstrate the performance of the heuristic algorithm, we assume an environment with 3 scenarios with a total of 8 tasks, where we generate random task graphs assuming random resources and requirements for PU types and tasks. The performance is estimated for different number of PU types and compared with a reference optimal solution obtained through CPLEX optimization solver. Figure 3 represents the normalized average energy consumption resulting from the heuristic with respect to the optimal optimizer, as well as the speed up in the execution time.

V. Conclusion

The paper proposes an energy aware static task mapping heuristic that considers static, dynamic, reconfiguration and communication energy. The heuristic provides solutions that are close to the optimal binary quadratic programming solution (within 20%) while achieving a speedup in the execution time up to three orders of magnitude compared to the optimal BQP.



(a) Heuristic vs. optimal



(b) Average normalized execution time

Fig. 3. Normalized performance and execution time

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