CPSC 330 Fall 2013 -- Exam 1 *<with answers>*

No calculators or other aids.

1. Give the power of 10 associated with these prefixes. (1.5 pts. each)

exa	_____	giga	_____	kilo	_____	mega	_____
micro	_____	milli	_____	nano	_____	peta	_____

<answers>

+18, +9, +3, +6
-6, -3, -9, +15

2. Define "benchmark program" and give at least one example. (3 pts.)

<suggested answer>

A program used to measure performance on a computer system, e.g., Dhrystone

3. Matching -- technology/performance terms. Write the correct term from the list into each blank. (1.5 pts. each)

embedded computer	datapath	throughput	arithmetic mean	Linpack
desktop computer	transistor	CPU time	harmonic mean	Whetstone
server	wafer	CPI	geometric mean	Dhrystone
supercomputer	yield	workload	speedup	SPEC

a. _____ a computer with highest performance and cost
b. _____ a computer that provides computation, file storage, and/or printing to multiple users across a network
c. _____ the circular slice of silicon upon which integrated circuits are built
d. _____ the ratio of the execution times of two computer systems
e. _____ used to summarize a set of normalized execution rates
f. _____ a set of benchmark suites that are used to compare the performance of various desktops and small servers

<answers>

supercomputer, server, wafer, speedup, geometric mean, SPEC

4. Give the CPU time equation and define the terms you use. (6 pts.)

<answer>

CPU time = IC * CPI * CCT

$$\text{or CPU time} = \frac{IC * CPI}{CR}$$

IC is instruction count
CPI is cycles per instruction
CCT is clock cycle time (which is equal to 1/CR)
CR is clock rate

5. Find the execution time for a program that executes 10 billion instructions on a processor with an avg. CPI of 2.5 and a clock frequency of 2 GHz. (6 pts.)

<answer>

$$\frac{(10 * 10^9 \text{ instructions}) * (2.5 \text{ cycles/instruction})}{2 * 10^9 \text{ cycles/second}} = 12.5 \text{ seconds}$$

6. For the following workload and cycle values, find the average CPI. (3 pts.)

type	freq	cycles
alu	0.2	1
ld/st	0.2	2
branch	0.6	4

CPI = _____

<answer>

CPI = .2*1 + .2*2 + .6*4 = 3

7. If a new compiler for the computer in question 6 could reduce the number of instructions to 1/2 of the original total and alter the instruction frequencies in the following manner, what would be the total speedup? (8 pts.)

type	freq	cycles
alu	0.5	1
ld/st	0.25	2
branch	0.25	4

<answer>

Note that there is a change in IC and CPI but not CCT.

New IC = 0.5 * original IC

New CPI = 0.5*1 + .25*2 + .25*4 = 2

$$\text{Speedup} = \frac{IC * CPI * CCT}{IC\_new * CPI\_new * CCT} = \frac{IC * 3 * CCT}{.5*IC * 2 * CCT} = 3$$

(note that IC and CCT cancel out, so you did not need to know their values)

8. Consider enhancing a scalar machine by providing a vector mode, which is 8 times faster than the normal mode of operation. If the percentage of vectorization is 60%, what is the overall speedup? (9 pts.)

<answer>

$$\text{Overall speedup} = \frac{1}{(1 - f) + \frac{f}{s}} = \frac{1}{.4 + .6/8} \rightarrow \text{simplifies to } 40/19$$

9. Matching -- logic terms. Write the correct term into each blank. (1.5 pts. each)

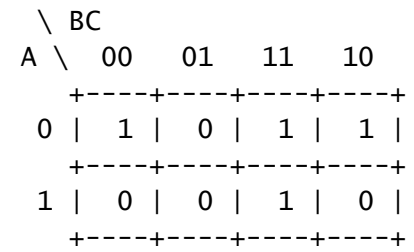
minterm	race condition	half adder	ALU	register
sum of products	circuit depth	full adder	PLA	shift register
don't care	fan-in	decoder	latch	RS latch
glitch	fan-out	multiplexer	flip-flop	JK flip-flop

a. _____ unused value that can be arbitrarily assigned 0 or 1
b. _____ undesired signal lasting only a short time
c. _____ a form of logical representation that employs a logical OR of product terms
d. _____ where the output of a circuit depends on small differences in signal timing
e. _____ the number of gates in a circuit that form the longest path from any input to any output
f. _____ a circuit in which n select values route one of 2**n input values to the single output
g. _____ a memory element in which the stored state can only change once per clock cycle
h. _____ a circuit that connects several flip-flops into a linear structure where the output of each flip-flop can be the input to either of its neighbors

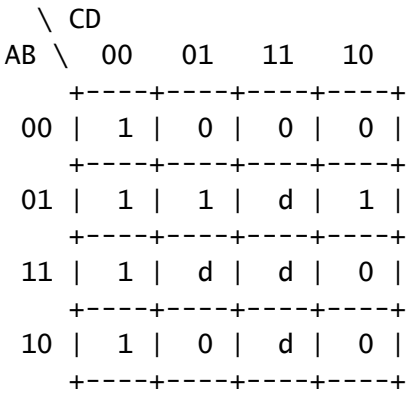
<answers>

don't care, glitch, sum of products, race condition,
circuit depth, multiplexer, flip-flop, shift register

10. Simplify the following Karnaugh maps of function F. (7 pts.)



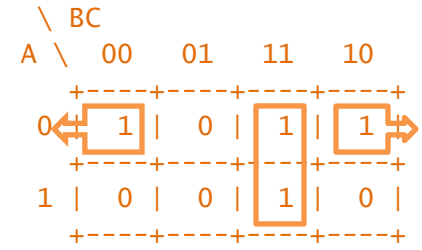
F = fn(A,B,C) = _____



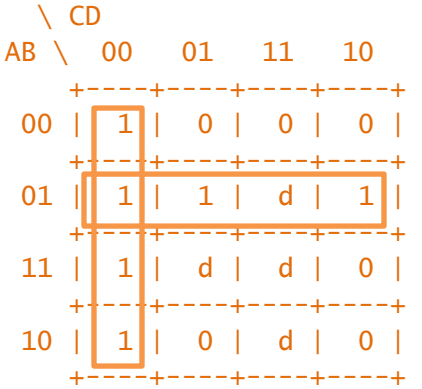
F = fn(A,B,C,D) = _____

d = don't care

<answers>



F = $\bar{A}*C + B*\bar{C}$

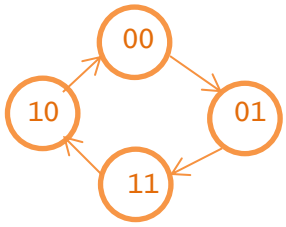


F = $\bar{A}*\bar{B} + C*\bar{D}$

11. Design a two-bit counter with the following repeated sequence: 0,1,3,2

(a) Give the state diagram. (3 pts.)
(b) Give the state transition table with current states QA(t) and QB(t), and next states QA(t+1) and QB(t+1). (3 pts.)
(c) Give the simplified logic expressions for QA(t+1) and QB(t+1). (3 pts.)

<answers>



QA(t)	QB(t)	QA(t+1)	QB(t+1)
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

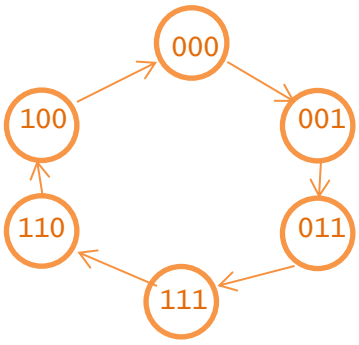
$QA(t+1) = QB(t)$

$QB(t+1) = \overline{QA(t)}$

12. Design a three-bit counter with the following repeated sequence: 0,1,3,7,6,4

(a) Give the state diagram. (4 pts.)
(b) Give the state transition table with current states QA(t), QB(t), and QC(t), and next states QA(t+1), QB(t+1), and QC(t+1). (4 pts.)
(c) Give the simplified logic expressions for QA(t+1), QB(t+1), and QC(t+1). (6 pts.)

<answers>



(unused states)

QA(t)	QB(t)	QC(t)	QA(t+1)	QB(t+1)	QC(t+1)
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	d	d	d
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	d	d	d
1	1	0	1	0	0
1	1	1	1	1	0

\ QB*QC

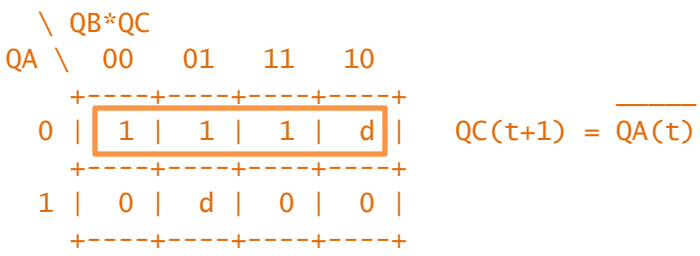
QA \	00	01	11	10
0	0	0	1	d
1	0	d	1	1

QA(t+1) = QB(t)

\ QB*QC

QA \	00	01	11	10
0	0	1	1	d
1	0	d	1	0

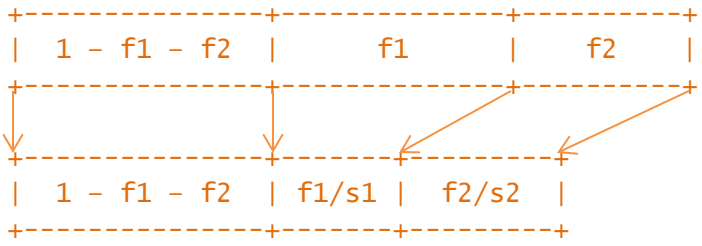
QB(t+1) = QC(t)



Extra Credit. (5 pts.)

Consider two independent enhancements with speedups s1 and s2, respectively. Let normal execution time be partitioned into a fraction f1 for which only the first enhancement is applicable, a fraction f2 for which only the second enhancement is applicable, and the remaining amount (1-f1-f2) for which neither are applicable. Note: there is no fraction of normal execution time in which both are applicable. Derive the overall speedup equation in terms of s1, s2, f1, and f2.

<answer>



$$\text{Overall speedup} = \frac{1}{(1 - f1 - f2) + \frac{f1}{s1} + \frac{f2}{s2}}$$