CPSC 3300 - Exam 1A - Spring 2016 Name: _____
No calculators.

1. Give the power of 10 associated with these prefixes. (1 pt. each)

exa _____ giga _____ kilo _____ micro _____ nano _____

2. Matching -- technology/performance terms. Write the correct term from the list into each blank. (1.5 pts. each)

embedded computer	datapath	throughput	speedup
desktop computer	transistor	CPU time	Whetstone
server	wafer	CPI	Dhrystone
supercomputer	die	workload	SPEC

a. _____ a computer used inside another device running one or more predetermined applications

b. _____ a semiconductor device used as a switch

c. _____ a round slice of silicon upon which integrated circuits are built during the manufacturing process

d. _____ the ratio of the execution times of two computer systems

e. _____ a synthetic benchmark for integer and system operations

f. _____ the component of the processor that contains registers, functional units, and internal busses

3. Find the execution time for a program that executes 60 billion instructions on a processor with an avg. CPI of 1.5 and a clock cycle time of 1 nsec. (8 pts.)

4. For the following workload and cycle values, find the average CPI. (5 pts.)

type	freq	cycles
alu	0.4	1
ld/st	0.4	4
branch	0.2	2

CPI = _____

5. If a processor redesign could reduce the CPI from 2.0 to 1.5 and increase the clock rate from 2.0 GHz to 3.0 GHz, what is the total speedup? (8 pts.)

6. What is the overall speedup in program execution time if an enhancement with a speedup of 6 is available and can be used to enhance 75% of the execution time? You should give you answer as a fraction. (6 pts.)

7. Matching -- logic terms. Write the correct term into each blank. (1.5 pts. each)

minterm	race condition	half adder	register
sum of products	circuit depth	full adder	PLA
don't care	fan-in	decoder	latch
glitch	fan-out	multiplexer	flip-flop

a. _____ unused value that can be arbitrarily assigned 0 or 1

b. _____ a form of logical representation that employs a logical OR of product terms

c. _____ the number of signals in a circuit that can be supplied as valid inputs from the output of a single gate

d. _____ a circuit in which n select values route one of 2**n input values to the single output

e. _____ a circuit in which two input values produce a sum and carry output

f. _____ a circuit that arranges several flip-flops into a common read/write structure with a single clocking signal

8. Simplify the following Karnaugh maps of function. (4 pts. each)

A \ BC	00	01	11	10
0	1	0	0	1
1	1	1	0	0

F = fn(A,B,C) = _____

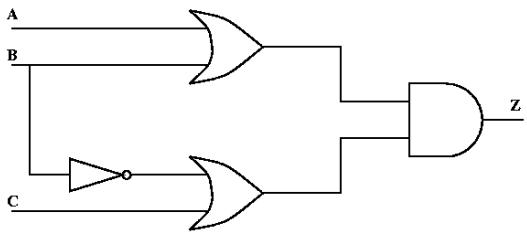
AB \ CD	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	0	0	0
10	1	1	1	1

F = fn(A,B,C,D) = _____

9. Give a circuit implementation for an XOR circuit using only AND, OR, and NOT gates. (5 pts.)

a	b	xor
0	0	0
0	1	1
1	0	1
1	1	0

10. Give a simplified logic expression for Z as a sum of products function of A, B, and C. (6 pts.)



11. Consider ~(A*B) = (~A) + (~B). Show by truth table that this is true.
    Remember to include the statement of equivalence. (5 pts.)

A	B	~A	~B	A*B	~(A*B)	(~A)+(~B)

12. Give simplified logic expressions for seven-segment display segments B and C.
    The final six rows (1010-1111) are don't cares for B and C. (5 pts. each)

Digit	Code	Segments						
	WXYZ	A	B	C	D	E	F	G
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	1	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1

13. Design a three-bit counter with the following repeated sequence: 0,1,3,5,7
    (a) Give the state diagram. (4 pts.)
    (b) Give the state transition table with current states QA(t), QB(t), and QC(t), and next states QA(t+1), QB(t+1), and QC(t+1). (6 pts.)
    (c) Give the simplified logic expressions for QA(t+1), QB(t+1), and QC(t+1). (6 pts.)

Extra Credit (up to 5 pts.)

Consider a function F to compare two two-bit fields, x1 x0 and y1 y0, and produce a one on output only if the two fields are the same. Consider using an FPGA CLB toimplement this function. Give the 16-bit LUT configuration where x1 x0 y1 y0 is the 4-bit input to the CLB. (Hint: x1*x0 + y1*y0 = 16'b0001000100011111 = 0x111f.)