CPSC 3300 – Spring 2016 – Exam 2 – Version A Name: _____

1. Matching. Write the correct term from the list into each blank. (2 pts. each)

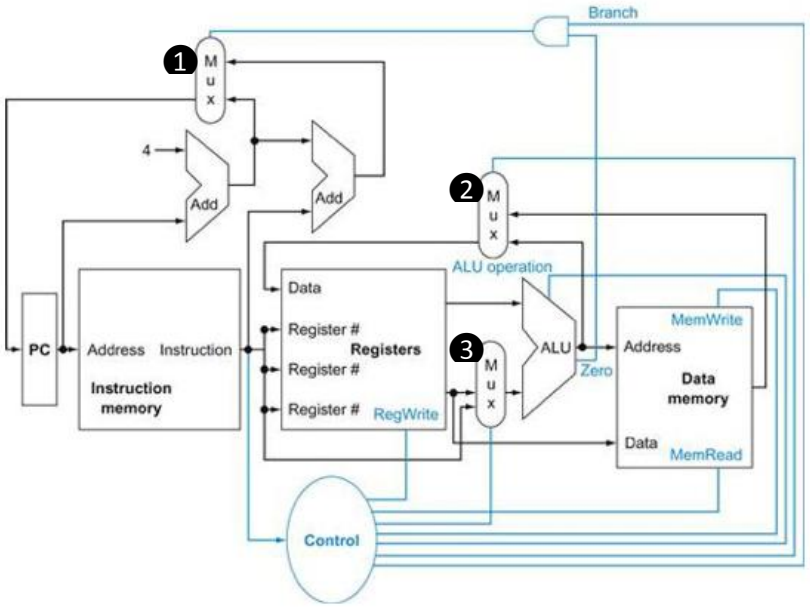
hardwired	structural hazard	control hazard	speculative execution
microprogrammed	load-use data hazard	forwarding	precise exception

(a) _____ generation of control signals from random logic or a PLA

(b) _____ generation of control signals from microinstructions fetched from a control store

(c) _____ providing a data value to any unit where it is needed after the data value has been produced but before it is available in the register file

(d) _____ allowing an instruction that is control dependent on a branch to execute after the branch direction is predicted and before the branch is resolved



2. Consider the MIPS "load word" instruction as implemented on the datapath above (Figure 4.2 from textbook):

lw R2, 8(R1) // Reg[2] <- memory[Reg[1] + 8]

Circle the correct value 0 or 1 for the control signals (a-d) and circle whether each of the three muxes (e-g) selects its upper input, lower input, or don't care. For the ALU operation (h) circle one of the function names. (The Zero condition signal will be assumed to be 0.) (16 pts.)

(a) Branch = 0 1

(b) MemRead = 0 1

(c) MemWrite = 0 1

(d) RegWrite = 0 1

(e) Mux1 (upper left; output to PC) = upper, lower, don't care

(f) Mux2 (upper middle; output to Data port of Regs) = upper, lower, don't care

(g) Mux3 (lower middle; output to bottom leg of ALU) = upper, lower, don't care

(h) ALU operation = and, or, add, subtract, set-on-less-than, nor

3. Identify the five stages of the simple scalar pipeline we studied, and explain what each stage does when processing the load instruction from question 2 above. (10 pts.)

```
lw   R2, 8(R1)   //  Reg[2] <- memory[ Reg[1] + 8 ]
```

4. Associate each term or statement below with a type of dependency. Circle one or more of RAW, WAR, or WAW. (Destination registers are listed first for add and subtract instructions.) (3 pts. each)

(a) RAW / WAR / WAW true data dependency

(b) RAW / WAR / WAW false data dependency

(c) RAW / WAR / WAW add R3,R1,R2 followed by sub R1,R3,R4

(d) RAW / WAR / WAW add R3,R1,R2 followed by sub R5,R3,R4

(e) RAW / WAR / WAW type of dependency that can cause a load-use penalty

5. Matching. Write the correct term from the list into each blank. (2 pts. each)

EPIC not an approach we studied superscalar VLIW

	dependency checking	***function unit assignment***	***execution scheduling***
(a) _____	hardware	hardware	hardware
(b) _____	hardware	software	software
(c) _____	software	hardware	hardware
(d) _____	software	software	software

6. Draw the dependency diagram for the following MIPS code. Destination registers are listed first except for the sw (store word) instructions; sw writes into memory rather than a register. (12 pts.)

```
lw    r2, 0(r1)
sw    r3, 0(r2)
add   r1, r2, r3
lw    r5, 4(r1)
add   r7, r5, r6
```

7. Give the pipeline cycle diagram (i.e., stairstep diagram) for the code segment given in question 6 above for the 5-stage pipeline with forwarding. (10 pts.)

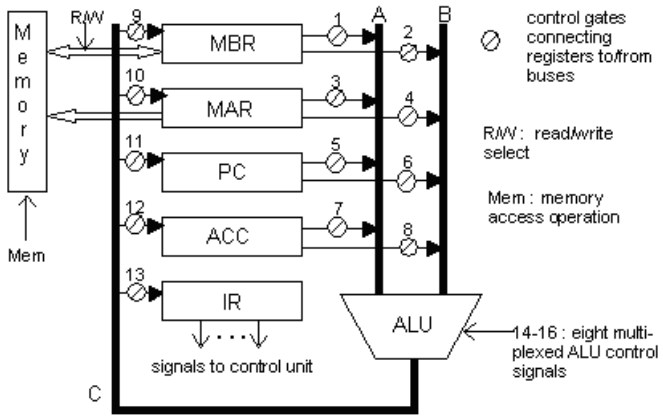
```
lw    r2, 0(r1)
sw    r3, 0(r2)
add   r1, r2, r3
lw    r5, 4(r1)
add   r7, r5, r6
```

8. The branch CPI penalty is calculated as extra CPI = (branch freq.)*(misprediction freq.)*(mispredict penalty)

(a) Which one of the three terms in the penalty equation will techniques like loop unrolling and predication reduce? (3 pts.)

(b) Which one of the three terms does dynamic branch prediction attempt to reduce? (3 pts.)

9. Consider the following datapath. (Assume all registers are edge-triggered and thus immune from races.) Control signal identifiers are given for the in and out control points of the registers. Additional control signals include memory signals Mem, R (read), W (write), and 3-bit ALU function field F.




```
ALU functions (three-bit F field)
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000: C = A + B     100: C = A - B
001: C = A         101: C = not A
010: C = A + 1     110: C = A - 1
011: C = A << 1    111: C = A >> 1
```

Complete the step-by-step RTL and the control signal sequence to fetch and execute a “store X” instruction. Assume that the instruction is composed of two memory words: a one-word opcode followed by a one-word address. Assume also that initially the address of the instruction is in the PC, and that the memory is word-addressable. The action of the instruction is memory[x] <- ACC, for the memory address X given in the second word of the instruction. (15 pts.)

// fetch opcode and place in IR	// control signals		
MAR <- PC	5 (A=PC),	F=001 (C=A),	10 (MAR=C)
PC <- PC + 1	5 (A=PC),	F=010 (C=A+1),	11 (PC=C)
MBR <- memory[MAR]	Mem, R		
IR <- MBR	1 (A=MBR),	F=001 (C=A),	13 (IR=C)

Extra Credit.

XC-1. Explain what the term BTB means and what the BTB component does in the P6 pipeline (see below). (5 pts.)

XC-2. Explain the purpose of the reorder buffer in the P6 pipeline. (5 pts.)