CPSC 3300 – Spring 2016 – Final Exam Version A – No Calculators Name: _____

1. Find the execution time of a program that executes 8 billion instructions on a processor with an average CPI of 2 and a clock frequency of 4 GHz. (3 pts.)

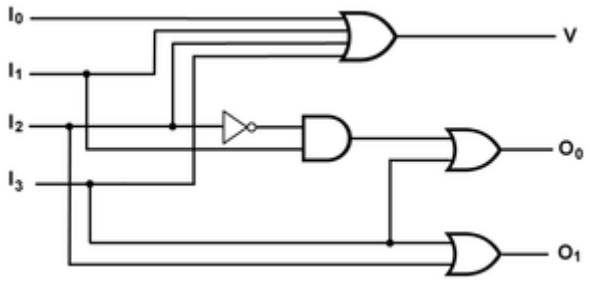
2. Use Amdahl's Law to determine the overall speedup if a performance enhancement with a six times speedup can be used 60% of the time. (3 pts.)

3. Why is the SPEC suite better than Dhrystone and Whetstone for benchmarking? (3 pts.)

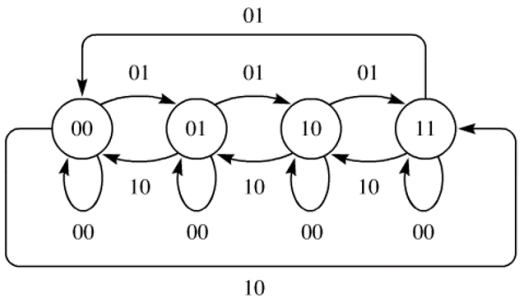
4. Give one of DeMorgan's Theorems (3 pts.), or alternatively give the distributive law for less credit (2 pts.).

5. Prove the theorem/law you gave for 4 above by truth table. (3 pts.)

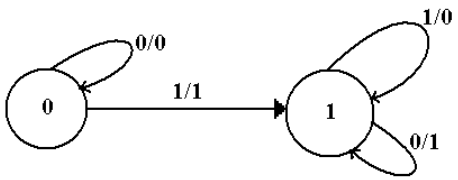
6. For the circuit below, give the logic expressions for V, O0, and O1. If the circuit represents a common type of combinational logic component, give the name of the component. (4 pts.)



7. What is missing in the following state diagram that makes it an incomplete specification of a state machine for sequential logic design? If the state diagram otherwise represents a common type of sequential logic component, give the name of the component. (2 pts.)



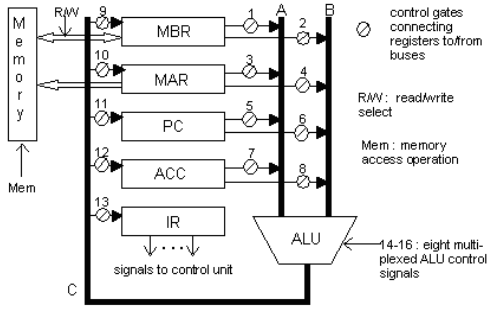
8. Give the truth table (i.e., state transition table) for the following state diagram. (5 pts.)



9. What is the advantage of a hardwired control unit? (3 pts.)

10. What is the advantage of a microprogrammed control unit? (3 pts.)

11. Consider the following datapath. Assume all registers are edge-triggered and thus immune from races. Control signal identifiers are given for the in and out control points of the registers. Additional control signals include memory signals Mem, R (read), W (write), and 3-bit ALU function field F.

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ALU functions (three-bit F field)
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000: C = A + B    100: C = A - B
001: C = A        101: C = not A
010: C = A + 1    110: C = A - 1
011: C = A << 1   111: C = A >> 1
```

Complete the step-by-step RTL and the control signal sequence to fetch and execute an indirect jump instruction "jmpi X". Assume that the instruction is composed of two memory words: a one-word opcode followed by a one-word address. Assume also that the address of the instruction is in the PC, and that the memory is word-addressable. The actions of the instruction are PC<-memory[X], for the memory address X given in the second word of the instruction. (8 pts.)

// fetch opcode and place in IR	// control signals		
MAR <- PC	5 (A=PC),	F=001 (C=A),	10 (MAR=C)
PC <- PC + 1	5 (A=PC),	F=010 (C=A+1),	11 (PC=C)
MBR <- memory[MAR]	Mem, R		
IR <- MBR	1 (A=MBR),	F=001 (C=A),	13 (IR=C)

12. Explain how you determine a true data dependency between two MIPS-like, register-to-register ALUop instructions (e.g., add, subtract). Which part(s) of each instruction is (are) used to determine the dependency? Give examples of a dependent pair of instructions and an independent pair of instructions. (6 pts.)

13. A reorder buffer provides for: (3 pts.)

a. branch misprediction recovery

b. precise exceptions even in the face of out-of-order completion of instruction execution

c. both a and b

d. neither a nor b

14. Identify at least three differences between DRAM and SRAM. (6 pts.)

15. Consider a computer system that contains a single-level cache with 2-nsec access time and a main memory with 40-nsec access time. If the hit rate is 75% and a cache miss requires both the initial cache access that determines the hit/miss and the subsequent memory access, what is the average memory access time (AMAT)? (4 pts.)

XC. Explain why write-invalidate is favored over write-update in most multiprocessor systems. (up to 5 pts.)

16. Consider these possible steps in cache access:

lookup using the index bits
refill (read cache line from memory)
route the correct line from one of the multiple banks
selection of bytes from the line using the offset bits
set the dirty bit
set the valid bit
tag match
write cache line back to memory if dirty

Write the steps in proper order for a read hit in a set-associative cache. (Note: some of the steps listed above may not be appropriate.) (4 pts.)

17. Give an example of accessing the elements of an array that illustrates temporal locality. (4 pts.)

18. Explain the 3C model of cache misses. Which types of misses does a fully-associative cache experience? (7 pts.)

19. Consider a 4 GiB byte-addressable main memory with a cache that is two-way set-associative, 64 KiB in size, and has a 32-byte line size.

(a) How many total lines are there in cache? (not just per bank) (2 pts.)

(b) How many lines are there in bank? (2 pts.)

(c) Show how the main memory address is partitioned into fields for the cache access and give the bit lengths of those fields. (6 pts.)

20. Assume a 256-byte main memory and a four-line cache with **two bytes per line**. The cache is initially empty. For the byte address reference stream given below, circle which of the references are hits for the different cache placement schemes. Also, show the final contents of the cache. (The byte addresses are in decimal.)

(a) 8-byte cache, direct-mapped, two bytes per line (8 pts.)

```
0,  11,  1,  2,  12,  3,  4,  13,  5,  6,  14, 7
```

(b) 8-byte cache, two-way set associative with LRU replacement, two bytes per line (8 pts.)

```
0,  11,  1,  2,  12,  3,  4,  13,  5,  6,  14, 7
```