CPSC 3300 Spring 2017 -- Exam 1 Name: _____

No calculators or other aids.

1. Give the power of 10 associated with these prefixes. (1 pt. each)

giga _____ kilo _____ mega _____ micro _____

milli _____ nano _____ pico _____ tera _____

2. Matching -- technology/performance terms. Write the correct term from the list into each blank. (1.5 pts. each)

embedded computer	datapath	throughput	arithmetic mean	Linpack
desktop computer	transistor	CPU time	harmonic mean	Whetstone
server	wafer	CPI	geometric mean	Dhrystone
supercomputer	chip	workload	speedup	SPEC

a. _____ a computer with highest performance and cost

b. _____ a computer that provides computation, file storage, and/or printing to multiple users across a network

c. _____ a measure of work per unit time

d. _____ the ratio of the execution times of two computer systems

e. _____ used to summarize a set of execution rates

f. _____ a synthetic floating-point benchmark, which today has more historical than practical value

3. Give the CPU time equation and define the terms you use. (6 pts.)

4. Find the execution time for a program that executes 6 billion instructions on a processor with an avg. CPI of 1.2 and a clock frequency of 3 GHz. (6 pts.)

5. For the following workload and cycle values, find the average CPI. (3 pts.)

type	freq	cycles
alu	0.2	1
ld/st	0.3	2
branch	0.5	4

CPI = _____

6. If a process shrink for the computer design in question 5 could increase the clock frequency from 2 GHz to 3 GHz and a new compiler could reduce the number of instructions to 2/3 of the original total and alter the instruction frequencies in the following manner, what would be the total speedup? (8 pts.)

type	freq	cycles
alu	0.5	1
ld/st	0.2	2
branch	0.3	4

7. Consider enhancing a scalar machine by providing a vector mode, which is 4 times faster than the normal mode of operation. If the percentage of vectorization is 50%, what is the overall speedup using Amdahl's Law? (8 pts.)

8. Matching -- logic terms. Write the correct term into each blank. (1.5 pts. each)

minterm	race condition	half adder	ALU	register
sum of products	circuit depth	full adder	PLA	shift register
don't care	fan-in	decoder	latch	RS latch
glitch	fan-out	multiplexer	flip-flop	JK flip-flop

a. _____ unused value that can be arbitrarily assigned 0 or 1

b. _____ undesired signal lasting only a short time

c. _____ a form of logical expression that is structured as the logical OR of product terms

d. _____ where the output of a circuit depends on small differences in signal timing

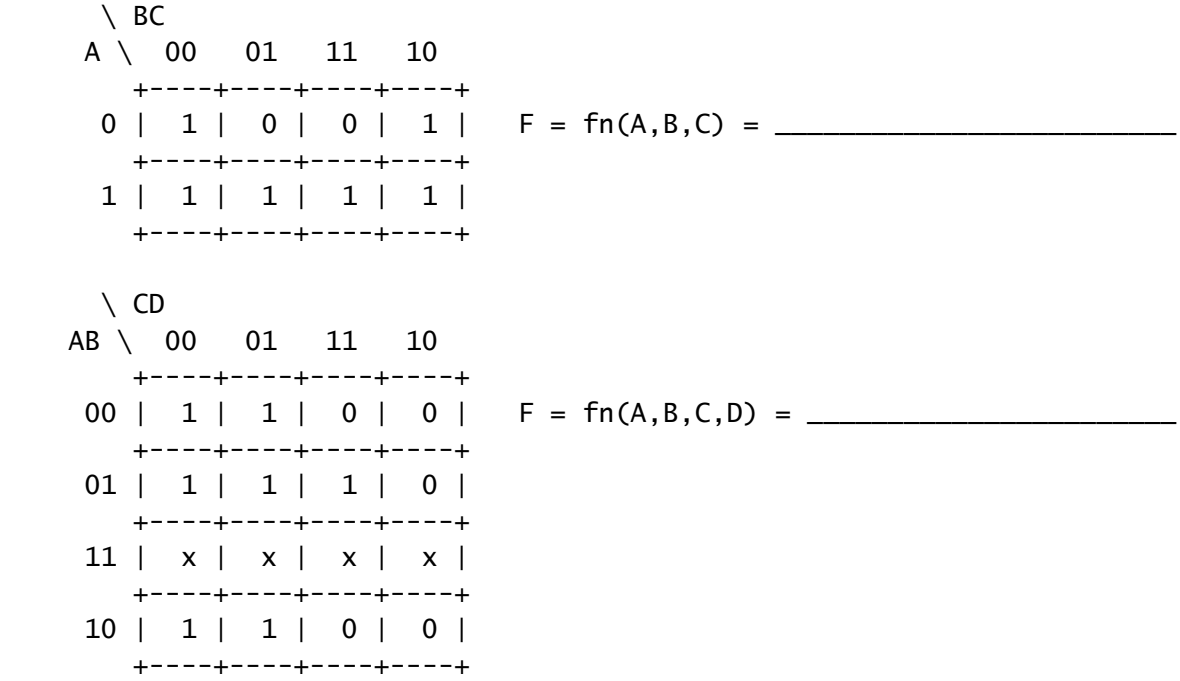
e. _____ the number of gates in a circuit that form the longest path from any input to any output

f. _____ a circuit in which n select values route one of 2**n input values to the single output

g. _____ a product term that contains all independent variables in either true or complemented form; it represents one row in a truth table

h. _____ a circuit that connects several flip-flops into a linear structure where the output of each flip-flop can be the input to either of its neighbors

9. Simplify the following Karnaugh maps of function F. (4 pts. each)



10. Consider A*((~A) + B) = A*B. Show by truth table that this is true. (7 pts.)
    (Hint: remember the final step in this type of proof!)

A	B	~A	~A + B	A*(~A+B)	A*B

11. Give a circuit implementation for an equality circuit using AND, OR, and NOT
    gates. (7 pts.)

a	b	equality
0	0	1
0	1	0
1	0	0
1	1	1

12. Design a three-bit counter with the following repeated sequence: 0,1,3,5,7
    (a) Give the state diagram. (4 pts.)
    (b) Give the state transition table with current states QA(t), QB(t), and QC(t), and next states QA(t+1), QB(t+1), and QC(t+1). (6 pts.)
    (c) Give the simplified logic expressions for QA(t+1), QB(t+1), and QC(t+1). (6 pts.)

XC. Let the following truth table define the effect that two inputs, R (reset) and I (input), have on a sequential circuit.

Q(t)	R	I	Q(t+1)
0	0	0	0
0	0	1	1
1	0	x	1
x	1	x	0

(a) Draw the state diagram for the table above. (5 pts.)

(b) Give the full table, with the don't cares expanded, and with J and K values needed to cause the appropriate state transitions on a JK FF. (6 pts.)

Q(t)	R	I	J	K	Q(t+1)

The JK excitation table is

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(c) Give K-maps for J and K and obtain a simplified logic expression for each. (4 pts.)