CPSC 3300 – Spring 2017 – Exam 2 Name: _____

1. Matching. Write the correct term from the list into each blank. (2 pts. each)

structural hazard	EPIC	forwarding	precise exception	hardwired
load-use data hazard	VLIW	control hazard	speculative execution	microprogrammed

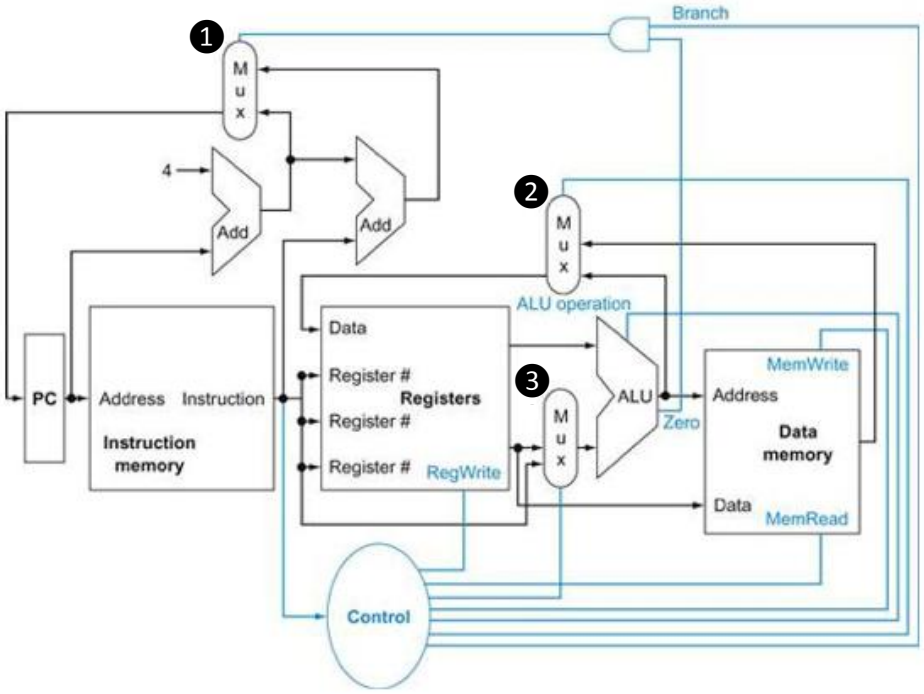
(a) _____ generation of control signals from random logic or a PLA

(b) _____ generation of control signals from microinstructions fetched from a control store

(c) _____ providing a data value to any unit where it is needed after the data value has been produced but before it is available in the register file

(d) _____ allowing an instruction that is control dependent on a branch to execute after the branch direction is predicted but before the branch is resolved

(e) _____ a type of instruction set architecture that groups multiple independent operations into a single wide instruction word, so that all operations in the instruction word are issued to function units at the same time.



2. Consider the MIPS "load word" instruction as implemented on the datapath above (Figure 4.2 from textbook):

lw R2, 8(R1) // instruction action is: Reg[2] <- memory[Reg[1] + 8]

Circle the correct value 0 or 1 for the control signals (a-d) and circle whether each of the three muxes (e-g) selects its upper input, selects its lower input, or is a don't care situation. For the ALU operation (h) circle one of the function names. (The Zero condition signal will be assumed to be 0.) (16 pts.)

(a) Branch = 0 1

(b) MemRead = 0 1

(c) MemWrite = 0 1

(d) RegWrite = 0 1

(e) Mux1 (upper left; output to PC) = upper, lower, don't care

(f) Mux2 (upper middle; output to Data port of Regs) = upper, lower, don't care

(g) Mux3 (lower middle; output to bottom leg of ALU) = upper, lower, don't care

(h) ALU operation = and, or, add, subtract, set-on-less-than, nor

3. Identify the five stages of the simple scalar pipeline we studied (in their correct order), and explain what each stage does when processing the load instruction from question 2 above. (10 pts.)

lw R2, 8(R1) // instruction action is: Reg[2] <- memory[Reg[1] + 8]

4. Matching. Write the correct term from the list into each blank. (2 pts. each)

BTAC dynamic VLIW EPIC predication superscalar VLIW

	dependency checking done by:	***function unit assignment done by:***	***execution scheduling done by:***
(a) _____	hardware	hardware	hardware
(b) _____	software	hardware	hardware
(c) _____	software	software	software

5. Explain why processors for servers, desktops, and laptops are typically superscalar rather than VLIW. (3 pts.)

6. Associate each term or statement below with a type of dependency. Circle one or more of RAW, WAR, or WAW. (Destination registers are listed first for add and subtract instructions.) (3 pts. each)

(a) RAW / WAR / WAW true data dependency

(b) RAW / WAR / WAW false data dependency

(c) RAW / WAR / WAW add R3,R1,R2 followed by sub R1,R3,R4

(d) RAW / WAR / WAW add R3,R1,R2 followed by sub R5,R3,R4

(e) RAW / WAR / WAW type of dependency that can cause a load-use penalty

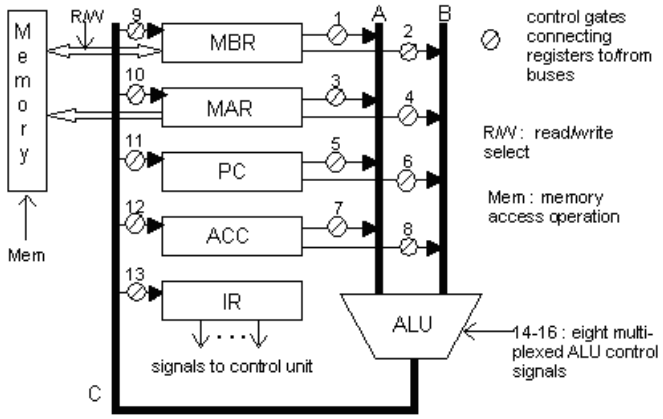
7. Draw the dependency diagram for the following MIPS code. Destination registers are listed first except for the sw (store word) instructions; sw has two source registers and writes into memory rather than a register. (10 pts.)

```
lw    r2, 0(r1)
sw    r3, 0(r2)
add   r1, r2, r3
lw    r5, 4(r1)
add   r7, r5, r6
```

8. Give the pipeline cycle diagram (i.e., stairstep diagram) for the code segment given in question 7 above for the 5-stage pipeline with forwarding. (6 pts.)

```
lw    r2, 0(r1)

sw    r3, 0(r2)

add   r1, r2, r3

lw    r5, 4(r1)

add   r7, r5, r6
```

9. Consider the following datapath. Assume all registers are edge-triggered and thus immune from races. Numeric control signal identifiers 1-13 are given for the “in” and “out” control points of the registers. Additional control signals include memory signals “Mem” (to enable a memory access), “R” (read select, causing MBR <- memory[MAR] when used in conjunction with Mem), “W” (write select, causing memory[MAR] <- MBR when used in conjunction with Mem), and a 3-bit ALU function field F (causing an action as shown in the table). A, B, and C are internal busses.




```
ALU functions (three-bit F field)
---------------------------------
000: C = A + B     100: C = A - B
001: C = A         101: C = not A
010: C = A + 1     110: C = A - 1
011: C = A << 1    111: C = A >> 1
```

Complete the step-by-step RTL and the control signal sequence to fetch and execute a “store X” instruction. Assume that the memory is word-addressable, that initially the address of the instruction is in the PC, and that the instruction is composed of two memory words: a one-word opcode followed by a one-word address. The action of the instruction is memory[X] <- ACC, where X is the memory address given in the second word of the instruction. (10 pts.)

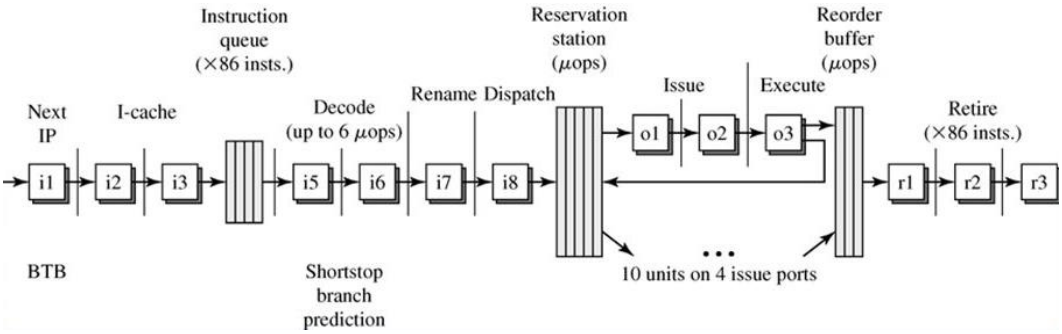
// fetch opcode and place in IR	// control signals		
MAR <- PC	5 (A=PC),	F=001 (C=A),	10 (MAR=C)
PC <- PC + 1	5 (A=PC),	F=010 (C=A+1),	11 (PC=C)
MBR <- memory[MAR]	Mem/R		
IR <- MBR	1 (A=MBR),	F=001 (C=A),	13 (IR=C)

10. Consider a one-bit history for branch prediction. It records the state of the last branch as taken (T) or untaken (U) and predicts the next branch will be the same. Assume the bit is initialized to U. Determine the prediction accuracy on the following branch traces of 20 observations each; include all 20 trace entries in your calculation. (3 pts. each)

(a) T T T T U T T T T U T T T T U T T T T U

(b) T U T U T U T U T U T U T U T U T U T U

11. Consider the first stage (i1) in the P6 pipeline depicted below. Explain what the acronym BTB means, and explain what the BTB component does (3 pts.)



12. Explain the purpose of the reorder buffer in the P6 pipeline, which is placed between stages o3 and r1. (5 pts.)

Extra Credit.

Here are the trace patterns given in question 10 but extended to 50 observations each:

(a) T T T T U T T T T U T T T T U T T T T U T T T T U T T T T U T T T T U T T T T U T T T T U T T T T U

(b) T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U T U

XC-1. How would a 2-bit saturating counter predictor improve prediction accuracy for the two trace patterns? Show a calculation of the accuracy. State your assumptions. (up to 6 pts.)

XC-2. How would a gshare predictor with a 2-bit BHSR and a PHT with 2-bit saturating counter predictors improve prediction accuracy for the two trace patterns? Show a calculation of the accuracy. State your assumptions. (up to 9 pts.)