Discussion at Nimbus Conf.
Dec 13, 1967
Gene Amdahl

	Busy	Duration
Single 32 bit	1/2 cycle	3/2
Double 64 bit	1	2

average

combined many 3 cycles

add

	Busy	Duration
Single	1/2	1 1/2
Double	2	3 1/2

repeat is half even though duration

mpy

Coronet is limited by adds
half can be single precision

32 bit is fixed, 64 slower than ACS 48 bit

Times: DTF code very tight 32 cycles in ACS

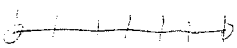
	ACS		NS6	
DTF	33/4 cycles	400 ns	296. ns	(all half cycle)
CORONET	33 cycles	412.5	288.	1st diff in Gaffle increments to

→ assume 8 floating point regs,
both assumed to fit in memory.

else Equivalence AD(J,K) AA(I), AB(I)

① word length? design used 32 not 64
½ of work is single precision

② branching: testing in advance?
overlapping of work one has to do on branching
ACS min time is 7 cycles to prepare to branch.

 14–21 instr

but many codes are every 4 instrs

for many branch / some branches / few branches — little gain / some gain / little gain

one can look for branches a little early
so gives most of gain

e.g. DTF 8 branches in loop
14 cycles more spent on branches.
(only 4 could have been removed)

skips

③ carefully use 4K words to avoid "load base regs"...
equivalence statements
interleaved arrays, etc. ← some can be done automatically.

optimization is easier than ACS, e.g. branches aren't moved ahead.

④ No. of registers:
RX instructions costs regs for HS regs to about ½, 8 regs is enough
ACS could use fewer regs — there is available time to store + refetch from memory
ACS needs 15 regs

⑤ 3 address. only 5% more reg to reg in practice.
more bits to address instructions not time

(6) ~~[illegible]~~
need not have ~~[illegible]~~ trap a la 91
or probably build in slow.

(7) competition. can't use this — satisfy growth of our customers

(8) 8K floating point: faster,
anomalies ~~[illegible]~~ are being fixed up

(9) OS is slow — investment can be
put into improving OS + it is there
rather than ACS new + getting better
system...

"85 I" compatible...

peak MIP rate 500 MIP.
(Can't sustain)

[2.7 X linear dimensions
still with 12.5 ns

(10) Level of Complexity...

(11) Multiple Instr. Counters?
They plan to offer 2 instr. counters. {cuts high speed reg. in half
equiv to 2 machines under one roof — lining losses
(many franchises are assumed) ~~[illegible]~~
are reduced by 1/4

built in HASP system

(provided not I/O limited)

(12) S/360 wasn't looked at ~~[illegible]~~ by ACS, it was Amdahl.
It does outreach the hardware cost in this case — [illegible] the whole machine [illegible]

conservative - safe design -- only way is guarantee perf.
for bad code situations ... branch area
a 2nd instr. ctr, will raise total.

NSG: smaller HS stor {20% shorter access time
early look at branches ... 40% less time rather than 20% for ACS.
1.4 X faster on bad code over ACS

averages of times (1/rates) not rates

Constant